a first impurity storage region containing said first conductivity type impurity, having one end connected to an end of said first gate electrode, and arranged in a direction different from the direction of arrangement of said first and second gate electrodes; and

a second impurity storage region, physically connected to said first impurity storage region by a semiconductor layer, said second impurity storage region containing said second conductivity type impurity, and having one end connected to an end of said second gate electrode, having the other end electrically connected to the other end of said first impurity storage region, and arranged in a direction different from the direction of arrangement of said first and second gate electrodes,

the widths of said first and second impurity storage regions are equal to the gate length of said first and second gate electrodes and the lengths of said first and second impurity storage regions are longer than said gate length.

C1

9. (amended) A semiconductor device as set forth in claim 1, wherein:

C2

said semiconductor layer is formed by polycrystalline silicon and said first and second gate electrodes and first and second impurity storage regions are formed by selectively implanting impurities to said polycrystalline silicon layer.

10. (amended) A semiconductor device as set forth in claim 1, wherein the width of said semiconductor layer physically connecting said first and second impurity storage regions is a value allowing mask misalignment when forming said first and second gate electrodes and first and second impurity storage regions.

REMARKS

The examiner rejected claims 9 and 10 under 35 U.S.C. § 112, second paragraph as indefinite, because they depend on a cancelled claim. As can be seen by the above amendments, the dependency of claims 9 and 10 have been changed, so that this ground for rejection has been overcome.